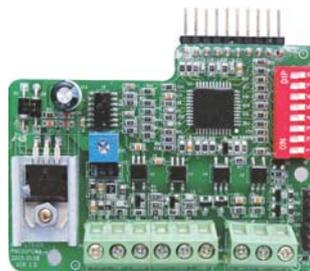




Operation Manual for PG Card



Option card for CHV series close loop vector control inverter

1. General Introduction

1.1 Functional Description:

If control mode is set to be vector control with PG, PG card will be a must to achieve this function. PG card includes power supply for encoder (+12V output which can be adjusted by the potentiometer on the PG card) and circuits for two channels of orthogonal encoder signals, which are capable of receiving signals from differential output, open collector output and push-pull output encoders. In addition, it can output frequency-division signal of input signals.

1.2 Dimensions and Installation

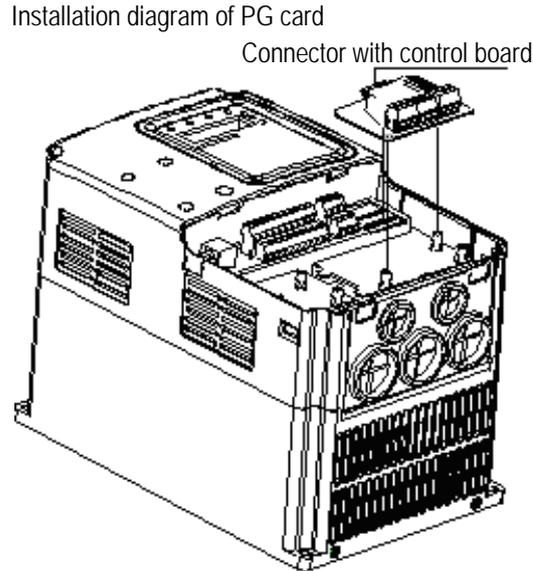


Figure 1.1 Installation of PG card

Outside dimensions and installation dimensions of PG card

Two PB3 × 10 tapping screws for PG card installation

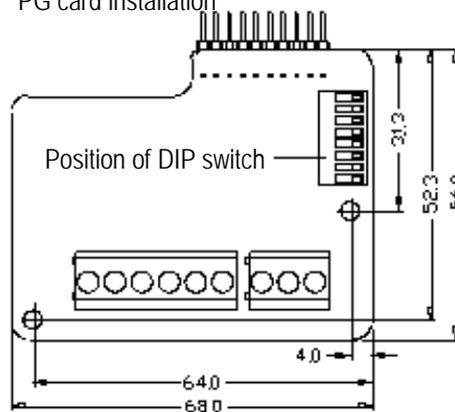


Figure 1.2 Dimensions of PG Card.

2. Operating Instructions

2.1 Technical Features

Terminal	Function	Response Speed	Output Impedance	Voltage Range	Output Current	Frequency Division Range
+12V, COM1	Encoder power supply	---	300Ω	12~16V	300mA	---
TERA+, TERA-, TERB+, TERB-	Encoder signal access	0~80 KHz	---	0-24V	---	---
TER-OA, TER-OB	Frequency division signal output	0~80 KHz	30Ω	---	100mA	1~256 (even number)

2.2 Description of Terminals and DIP Switch

+12V and COM1: Power supply for encoder.

TERA+, TERA-, TERB+, and TERB-: Signal input terminals for encoder.

TER-OA, TER-OB, and COM1: Output terminals for frequency-division signals.

PE: Wiring terminal for shielding cable (user should connect it to the ground).

The frequency division factor is determined by DIP switch on PG card. DIP switch consists of 8 bits. The frequency division factor will be determined by binary number which is selected by combination of 8 bits. The bit marked as "1" on the DIP switch is the lowest binary bit, while "8" is the highest binary bit. When the DIP switch is switched to ON, the bit is valid, indicating "1"; otherwise, it indicates "0".

Frequency division factors are shown in the below table:

Decimal Number	Binary Bit	Frequency Division Factor
0	00000000	1
1	00000001	2
2	00000010	3
...
m	...	m+1
255	11111111	256

2.3 Wiring Diagram

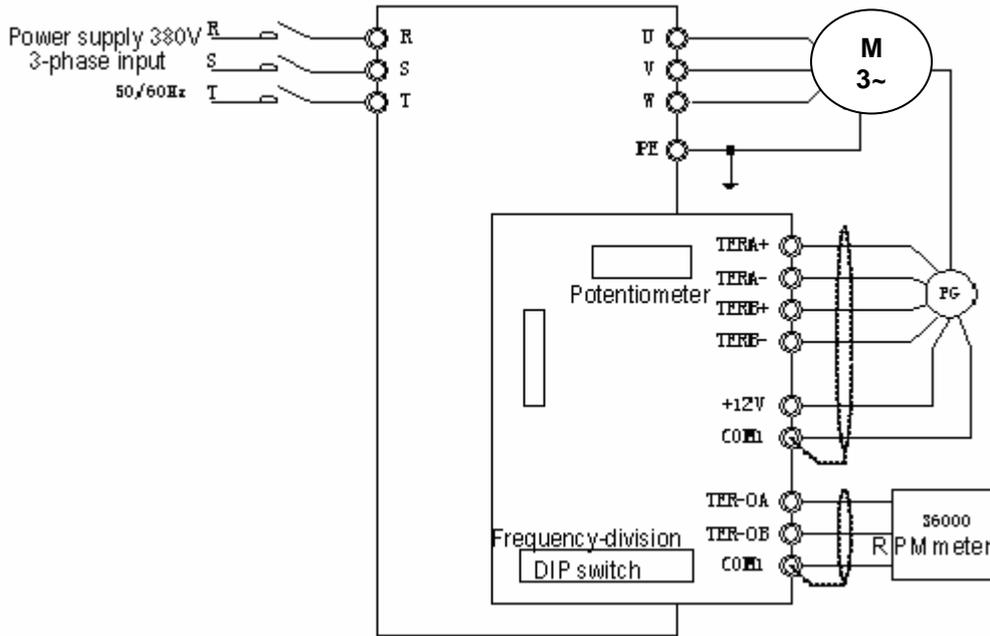


Figure 2.2 Wiring Diagram.

Notice:

- Wire of PG card should be separated from power supply wire. Parallel wiring is forbidden.
- To prevent encoder signals from disturbance, please select a shielded cable as the signal wire of PG card.
- The shielding layer of shielded cable of PG card should be grounded one end to prevent signal from disturbance.
- If the frequency-division output of PG card is connected to external power supply, the voltage should be less than 24V; otherwise, the PG card may be damaged.

3. Typical Connection

3.1 Wiring diagram of differential output

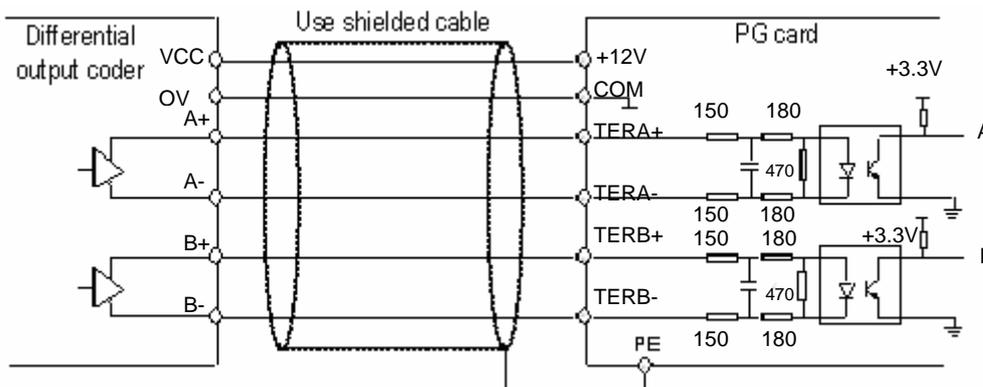


Figure 3.1 Wiring diagram of differential output

3.2 Wiring diagram of open collector output

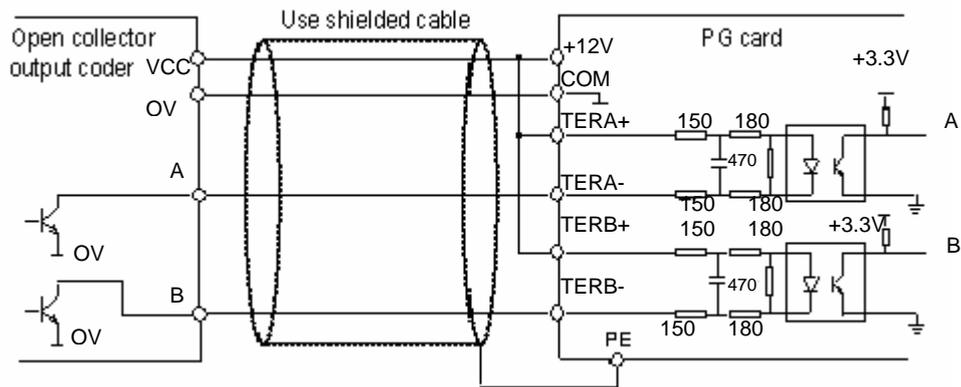


Figure 3.2 Wiring diagram of open collector output

3.3 Wiring diagram of push-pull output

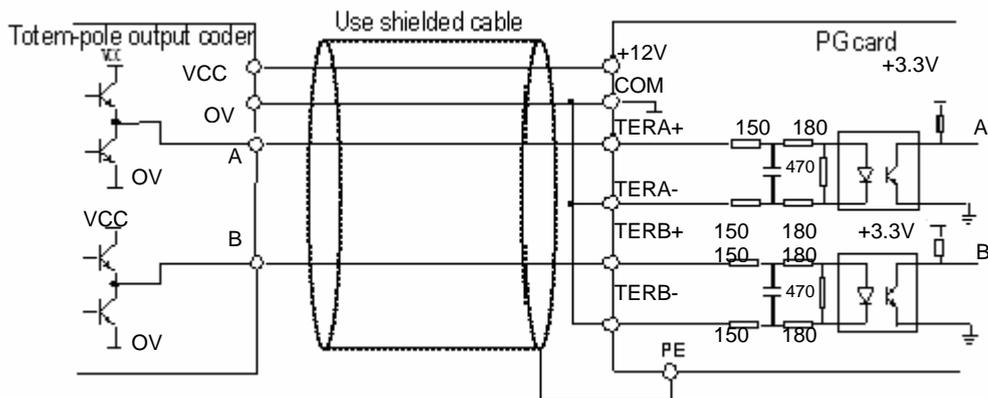


Figure 3.3 Wiring diagram of push-pull output

3.4 Wiring diagram of frequency-division output

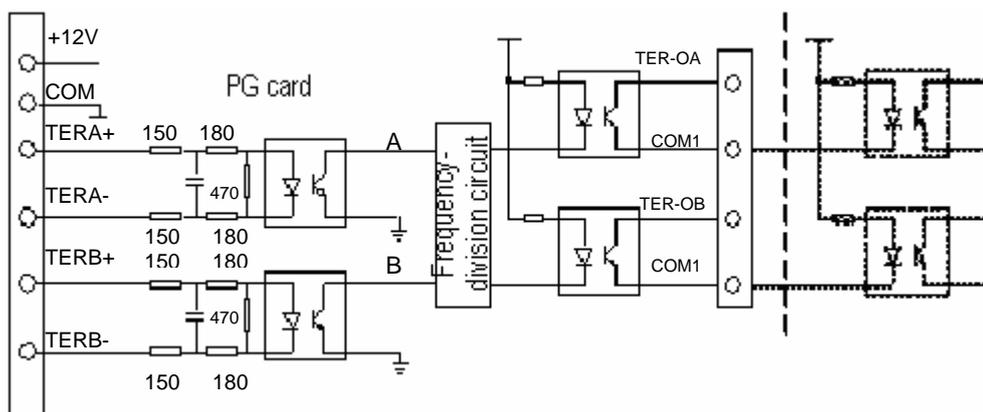


Figure 3.4 Wiring diagram of frequency-division output.